Strathmore UNIVERSITY

SCHOOL OF COMPUTING AND ENGINEERING SCIENCES
BACHELOR OF ELECTRICAL AND ELECTRONICS ENGINEERING
END OF SEMESTER EXAMINATION

BEE 3102: DIGITAL ELECTRONICS II

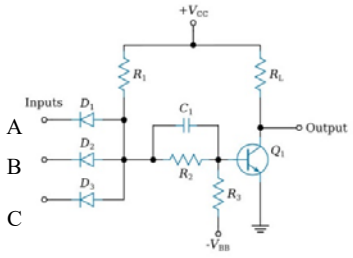
DATE: 31st July 2023 **Time: 2 Hours**

Instructions

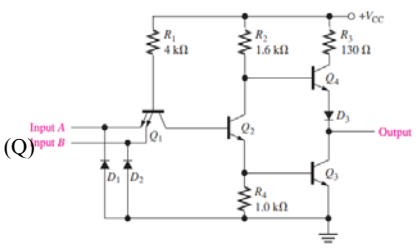
1. This examination consists of **FIVE** questions.
2. Answer **Question ONE (COMPULSORY)** and any other **TWO** questions.
3. Do not write on the question paper.

QUESTION ONE **(Total:30 Marks)**

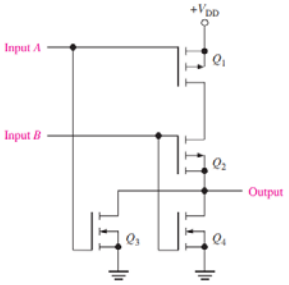
a) Develop the truth tables for the following logic families' circuits and state their respective logic families. (6 Marks)



1a



1b



1c

Figure 1: figure 1a (2 marks), figure 1b (2 marks), figure 1c (2 marks)

b) Design a sequential decoder circuit (lighting circuit) with two JK Flip-Flops, A and B, and one input x. The states S_0, S_1, S_2, and S_3 represents red, green, blue, and white lights with state assignments as 00, 01, 10, and 11 respectively. When x = 0, the state of the circuit remains the same. When x =1, the circuit goes through the state transitions from red to green to white to blue and back to red, and repeats. *(Hint: develop a state graph, excitation table, flip flop equations, and logic circuit).* (10 Marks)

c) A 10-bit DAC has a step size of 10 mV. Determine the full-scale output voltage and the percentage resolution. (4 Marks)

d) Minimize the number of states in figure 2 using implication tables and redraw the minimized state graph. *Show all the steps.* (6 Marks)

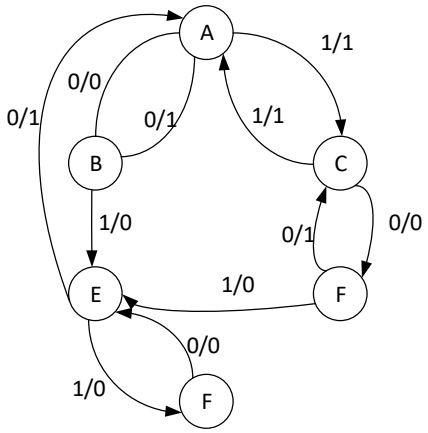


Figure 2: State Graph

e) Using a diagram, differentiate between Moore and Mealy machine. (4 Marks)

QUESTION TWO **(Total: 15 Marks)**

a) A given sequential network has one input and one output. The output becomes 1 and remains 1 thereafter when at least two zeros and at least two ones have occurred as inputs, regardless of the order of occurrence. Draw a state graph (Moore type) for the network. *Note: 9 states are sufficient and your final state graph should be neatly drawn with no crossed lines.* (4 Marks)

b) A four piston car engine must to go through four strokes namely; intake, compression, power, and exhaust, all of equal duration resulting in a state sequence as shown in Figure 3. On the first stroke the inlet valve is open and the outlet is closed; on the second stroke the inlet is closed and compression occur; on the third stroke a spark is delivered leading to rotation by the crankshaft; and at the forth stroke, the outlet is open for the exhaust from the explosion to vent. Then the first stroke comes again and the cycle repeats. Your work is to design a controller for the system, with a clock for input and with three outputs: one to open the inlet, one to open the outlet, and one to ignite the spark. Assume that if the control to open a valve isn't asserted, the valve closes (spring-loaded valve). The frequency of the clock will determine the speed of engine. The design should be based on the following questions.

i. Determine the number of flip-flops required and the type of coding scheme to use. (1 Mark)
ii. Develop a state table for the system. (2 Marks)
iii. Develop the excitation table. (2 Marks)
iv. Using Karnaugh maps, determine the flip-flop inputs equations and the output combinational logic. (3 Marks)
v. Draw the resulting circuit diagram (3 Marks)

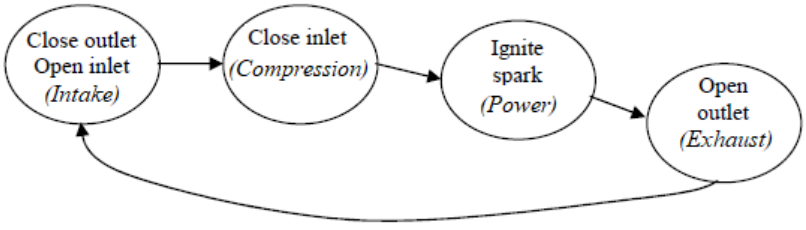


Figure 3: State Sequence of Engine Cycle

QUESTION THREE **(Total: 15 Marks)**

a) Implement the following two Boolean functions with a PLA: *Show all the steps.* (7 Marks)

$F_1(A, B, C) = \sum m(1, 2, 4)$ and $F_2(A, B, C) = \sum m(5, 6, 7)$

b) Determine the output of the DAC in Figure 4 if the sequence of 4-bit numbers in part (b) is applied to the inputs. The data inputs have a low value of 0 V and a high value of +5 V. *show all the steps.* (8 Marks)

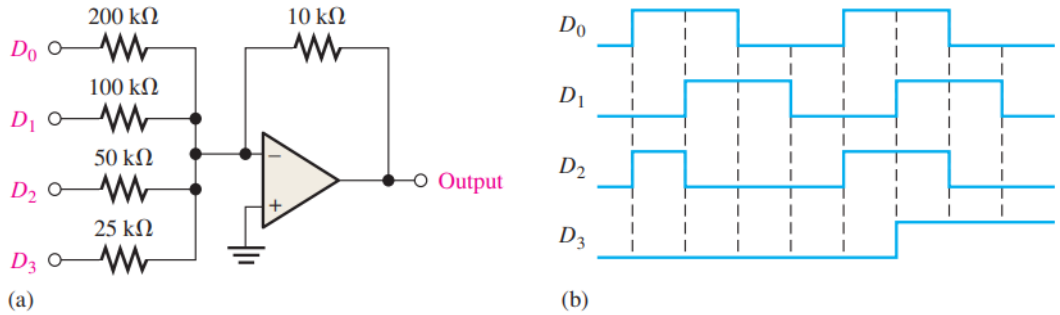


Figure 4

QUESTION FOUR **(Total: 15 Marks)**

a) Using clearly labelled block diagrams, differentiate between Programmable Read Only Memory (PROM), Programmable Array Logic (PAL), and Programmable Logic Array (PLA). (3 Marks)

b) Figure 4 below shows a sequential circuit with various delays.

i. Briefly define the 4 timing parameters used in sequential circuits (4 Marks)
ii. What is the minimum clock period (T_{min}) of this circuit? (2 Marks)
iii. What is the maximum clock frequency F_{max}? (2 Marks)
iv. Validate Flip-Flop hold time (2 Marks)
v. Draw the timing diagram (2 Marks)

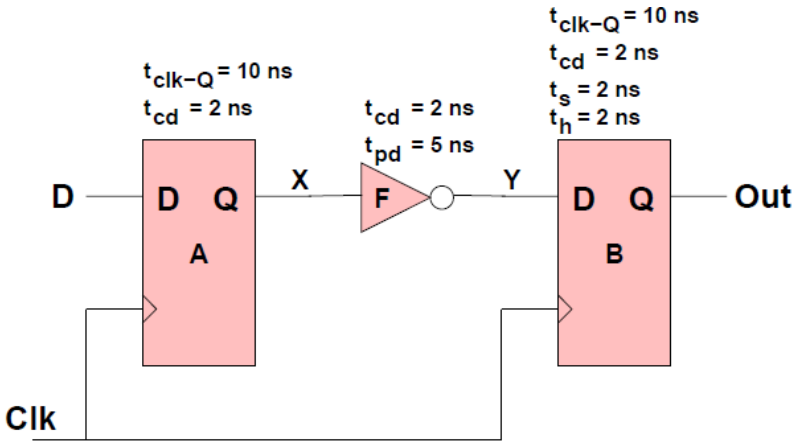


Figure 1: Delays in a Sequential Circuit

QUESTION FIVE **(Total: 15 Marks)**

a) For the given state diagram in Figure 7;

i. Determine the type of machine. (½ Mark)

ii. Determine the sequence that is detected. (1 Mark)

iii. Determine the case of detection. (½ Mark)

iv. Draw the state table. (2 Marks)

v. Using the state assignment S0=00, S1=01, S2=10, S3=11 draw the state table with assignment. (1 Mark)

vi. Determine the number of flip-flops required. (½ Mark)

vii. Draw the excitation table using D flip-flops determine the flip-flops excitation expressions/equations. (3½ Marks)

viii. Draw the logic circuit. (2 Marks)

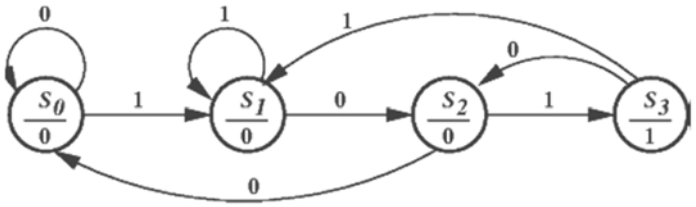


Figure 7

b) Write the Verilog code that implements the scenario in question 5a above. (4 Marks)