Strathmore UNIVERSITY

School of Computing and Engineering Sciences

Bachelor of Science in Electrical and Electronics Engineering

End of Semester Examination

BEE2201: Digital Electronics I

Date: 6TH March 2024 **Time 08:00-11:00 Hours**

Instructions: Answer Question **ONE** and any other **TWO** Questions

Question ONE (30 Marks)

a) Convert the following to the base indicated

i. $(1001.0101)_2$ to decimal 1 Marks

ii. $(13.375)_{10}$ to binary 1 Marks

iii. $(73.75)_{10}$ to Octal 1 Marks

iv. $(762.013)_8$ to Hexadecimal 1 Marks

b) Perform the following operation using 2's complement method

i. $(37)_{10} + (-18)_{10}$ (2 Marks)

ii. Subtract $(-64)_{10}$ from $(32)_{10}$ (2 Marks)

c) Simplify the following Boolean expression using Boolean laws

i. $Y = AB + A'B + AB' + (AB)'$ (2 Marks)

ii. $X = A' + ABC + A(B \oplus C) + AB'C'$ (2 Marks)

d) Obtain the minterm expansion for F(A,B,C) in fig.1 below (2 Marks)

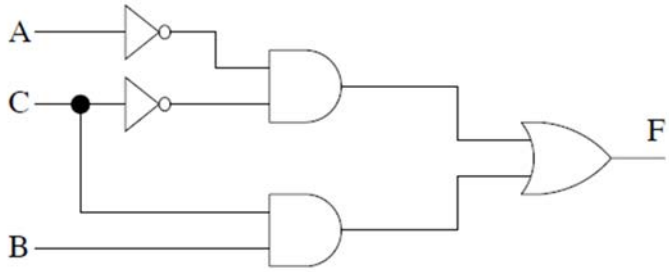


Fig. 1

e) For a given Boolean function F(A,B,C,D)=∑(0,2,5,7,10,13,15) which has don't care conditions d(A,B,C,D)=∑(4,8,14).

i. Simplified the Boolean function using Karnaugh Map. (2 Marks)

ii. Implement F with only NAND gates (2 Marks)

f) Implement a full adder circuit using 3 to 8-line decoder. (4 Marks)

g) The 100kHz square waveform of fig 2(a) below is applied to the clocked input of the flip-flop shown in fig 2(b). If the Q output is initially '0',

i. Draw the output Q waveform. (1 Mark)

ii. Determine the frequency of the Q output (1 Mark)

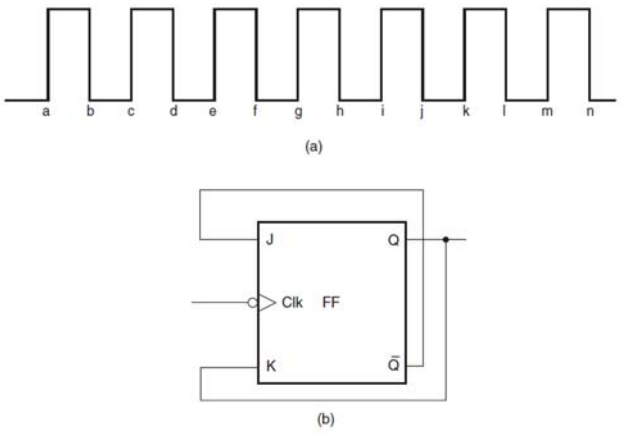


Fig. 2

h) Show how to implement two input OR gate using NOR gates (2 Marks)

i) Draw the logic diagram of a 4-bit serial in serial out shift register using JK flip-flops and explain its working with an example. (4 Marks)

Question TWO (15 Marks)

a) A 4-bit binary number is applied to a circuit on four lines A, B, C, and D. the circuit has a single output, F, which is true if the number is in the range of four to eleven, inclusive.

i. Draw a truth table to represent the problem (3 Marks)

ii. Use the K-map to obtain a simplified expression for the function (3 Marks)

iii. Construct a circuit to implement the simplified expression in (ii) above using NAND gates only (3 Marks)

b) Briefly explain the following terms: -

i. Registers (1 Mark)

ii. Shift-registers (1 Mark)

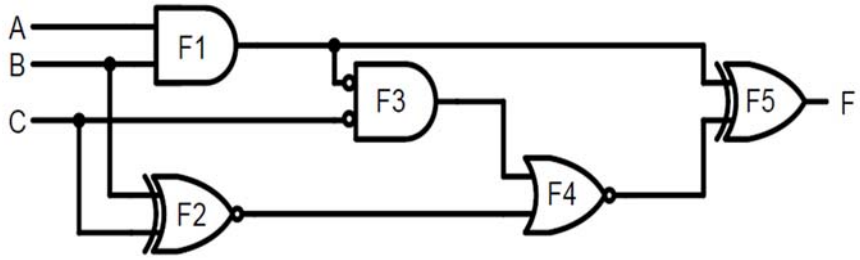
c) With the aid of logic symbols and truth tables, explain the operation of the following two-input gates.

i. NOR (2 Marks)

ii. XOR (2 Marks)

Question THREE (15 Marks)

a) Analyze the following circuit



i. Obtain the Boolean expression for the output (F) (4 Marks)

ii. Use the truth table and determine the output F as sum of minterms and product of maxterms (4 Marks)

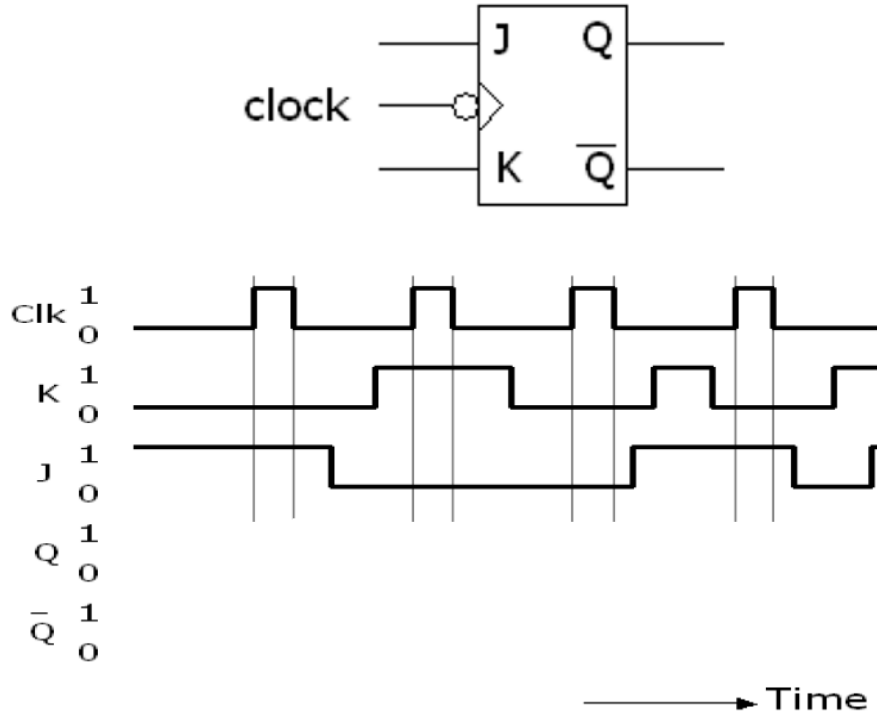
iii. Use Karnaugh Map to simplify the equation obtained in (i). (3 Marks)

iv. Implement the SOP and POS circuits with minimum number of gates. (4 Marks)

Question FOUR (15 Marks)

a) Design a combinational circuit that accepts a four bit number (A,B,C,D) and generates an output which is equal to the sum of the binary numbers formed by the input (AB) and (CD). (10 Marks)

b) Complete the given timing diagram for the circuit shown below (5 Marks)



Question FIVE (15 Marks)

a) The logic diagram of Fig. 1 performs the function of a very common arithmetic building block. Identify the logic function. (5 Marks)

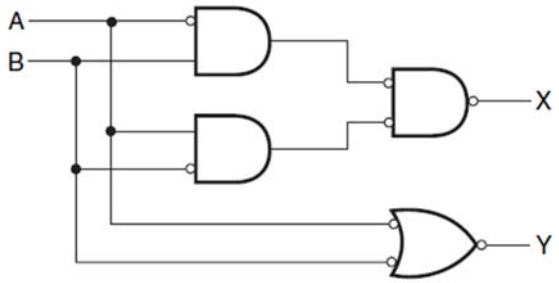


Fig. 1

b) Design modulus 12 asynchronous counter with a straight binary sequence from 0000 through 1011 using J-K flops. Draw the circuit diagram and associated timing diagram. (10 Marks)