Strathmore
UNIVERSITY

SCHOOL OF COMPUTING AND ENGINEERING SCIENCES
BACHELOR OF SCIENCE IN INFORMATICS & COMPUTER SCIENCE
END OF SEMESTER EXAMINATION
ICS2104/CNS 2202: COMPUTER ORGANIZATION AND ARCHITECTURE

DATE:28th July, 2023 Time: 2 Hours

Instructions

1. This examination consists of **FIVE** questions.
2. Answer **Question ONE (COMPULSORY)** and any other **TWO** questions.

Question 1 (30 Marks)

a. In the last four decades, computer design has been driven by the so-called "Moore's Law." This observation has seen computers double their speeds through the incorporation of more transistors in processing chips. However, there is a known limit for how small transistors can be made before affecting their effective performances; which begs the question: How will future computers be designed once this threshold limit is reached? Answer this question by suggesting two other ways computers can be designed and improved without increasing the number of transistors in a processing chip. **(5 Marks)**

b. Using the example of the hexadecimal numbers 0x12345678, highlight the difference between "***Big Endian***" and "***Little Endian***". **(4 Marks)**

c. Using an example, highlight the difference between Reduced Instruction Set Computer and Complex Instruction Set Computer? **(4 Mark)**

d. Using simple diagrams, show simple Turing Machines that perform any two arithmetic operations. **(3 Marks)**

e. There exist differences between the processor and memory locations speeds that progressively decreases as one moves away from processor. For optimal performance, cache replacement schemes have been employed to improve performances so that the processor is not idle most of the time.

   i. Explain any three cache replacement algorithms for memory blocks of data brought to the caches that services the processor. **(3 Marks)**

ii. Further, explain the choice of the most effective algorithm often used and why **(1 Mark)**

f. Draw an instruction cycle diagram with interrupts and discuss the instruction cycle process and the handling of interrupts **(5 Marks)**

g. Solid State Drives (SDD) have over time progressively replaced Hard Disk Drives (HDD) in use as storage devices. Explain any THREE advantages SDD has over HDDs. **(3 Marks)**

h. Explain any two design issues that affect the Instruction lengths or sizes. **(2 Marks)**

Question 2 **(15 Marks)**

a. Explain the concepts of temporal locality and spatial locality of reference in cache memory. **(2 Marks)**

b. Assume a disc has the following specifications: 2000 tracks; 100 sectors/track; and 8192 bytes/sector. How many bytes of information can be stored on this disc? **(4 Marks)**

c. Consider the cache memory for the following questions:

i. Why is the cache memory partitioned in to the Instruction/Code-Cache and the Data-cache? **(1 Mark)**

ii. Describe in detail the cache mapping techniques. **(5 Marks)**

d. Convert the infix expression (2+3) - 6/3 to postfix **(3 Marks)**

Question 3 **(15 Marks)**

a. Describe the stored program concept when applied to the Von Neumann model. **(4 Marks)**

b. A given computer has a single cache memory (off-chip) with a 2 ns hit time and a 98% hit rate. Its main memory has 40 ns access time.

i. What is the computer's effective access time? **(2 Marks)**

ii. If an on-chip cache with a 0.5 ns hit time and a 94% hit rate is added to it, what is the computer's new effective access time? **(2 Marks)**

iii. How much of a speedup does the on-chip cache give the computer? **(2 Marks)**

c. What is the difference between maskable and nonmaskable interrupts? **(3 Marks)**

d. What does it mean to say that the memory is 133MHz and the processor is 1.4 GHZ? **(2 Marks)**

Question 4 **(15 Marks)**

a. Both hard and soft errors are clearly undesirable in semiconductor memories. Often various algorithms are used to detect and correct these errors. Draw a simple illustration and explain how error handling codes function. **(5 Marks)**

b. A given hypothetical machine has two I/O instructions:

0011 Load AC from I/O
0011 Store AC to I/O

Where, the 12-bit address identifies a particular I/O device. Using the format given in Table 2, show the program execution for the following program:

1. Load AC from device 5.
2. Add contents of memory location 940.
3. Store AC to device 6.

Assume that the next value retrieved from device 5 is 3 and that location 940 contains a value of 2. **(5 Marks)**

Table 1

300	3005
301	5940
302	7006
.	
.	
.	
940	0002
941	

c. Briefly discuss TWO characteristics used to classify computer memory systems. **(2 Marks)**

d. Define the terms: Seek Time, Rotational Delay and Access Time **(3 Marks)**

Question 5 **(15 Marks)**

a. Consider two different machines, A & B, with two different instruction sets, both of which have a clock rate of 200 MHz. The measurements in Table 2 are recorded on the two machines running a given set of benchmark programs:

Table 2

Instruction Type	Instruction Count (I_c) (millions)		Cycles per Instruction (CPI)	
	A	B	A	B
Arithmetic and Logic	8	10	1	1
Load and Store	4	8	3	2
Branch	2	2	4	4
Others	4	4	3	3

i. Determine the effective CPI, million instructions per second (MIPS) rate, and execution time (CPU) for each machine. **(12 Marks)**

ii. Comment on the results. **(1 Mark)**

b. Briefly describe George Amdahl's law on the speed up of computer components. **(2 Marks)**