Strathmore
UNIVERSITY

SCHOOL OF COMPUTING AND ENGINEERING SCIENCES
BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING
END OF SEMESTER EXAMINATION
BEE 2201: INTRODUCTION TO DIGITAL ELECTRONICS

DATE: 7th December 2022 Time: 3 Hours

Instructions

1. This examination consists of **FOUR** questions.
2. Answer **QUESTION ONE** and any other **TWO QUESTIONS.**

Question 1 (30 Marks)

(a) Draw logic circuits and show how you can implement the logical AND and logical OR using only;

(i) NAND gates 2 Marks

(ii) NOR gates 2 Marks

(b) Convert the following to the base shown;

(i) $(2D3.5)_{16}$ to base 10 2 Marks

(ii) $(.3125)_{\mathbf{10}}$ to base 8 2 Marks

(iii) $(3A9F)_{16}$ to base 2 2 Marks

(iv) $(3A9F)_{16}$ to base 8 2 Marks

(c) Use binary arithmetic to compute $(5)_{10} - (12)_{10}$ using 2's complement and express the results in signed base 10 format. 4 Marks

(d) Use a truth table to proof by induction DeMorgan's theorem $\overline{(A + B)} = \overline{A}.\overline{B}$ 4 Marks

(e) Simplify the expression z = $\left(\overline{A} + C\right).(B + \overline{D})$ 4 Marks

(f) Fig. Q1(f) shows the truth table where z is the desired output logic function. Express the logic function z as a Sum Of Products and draw a circuit to show how you can use an 8-to-1 multiplexer to implement the SOP for the logic function z. 6 Marks

C	B	A	z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Fig. Q1(f) Truth Table for logic function z

Question 2 (15 Marks)

Fig. Q2 shows the truth table for a full adder implementation for adding two bits A_i B_i and carry input C_{in} with output sum S_i and carry output C_{out}

(i) Reduce the sum S_i into an XORs representation. 5 Marks

(ii) Show that $C_{out} = A_iB_i + C_{in}(A_i \oplus B_i)$ 5 Marks

(iii) Draw a circuit diagram to show a full binary adder implementation using two half adders. 4 Marks

(iv) What is the is the definition of overflow in 2's complement addition. 1 Mark

C_{in}	A_i	B_i	S_i	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig. Q2 Full Adder Truth Table

Question 3 (15 Marks)

(a) Fig. Q3(a) shows the clock and signals S, R which are applied to the inputs of an SR Latch. Draw the Gated SR Latch NAND gates implementation and sketch the waveforms Q and $\overline{Q}$ 4 Marks

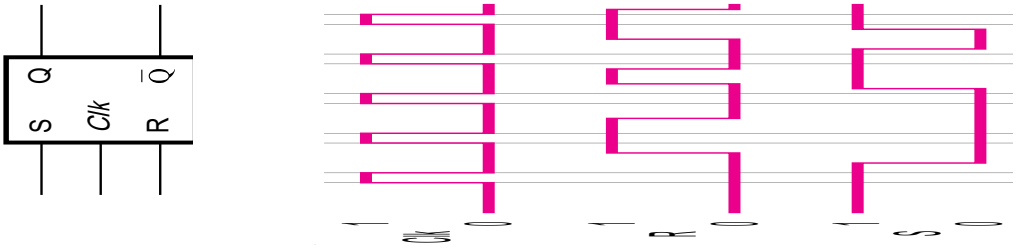
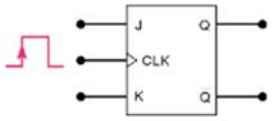


Fig. Q3(a) SR Flip Flop

(b) For the JK flip shown in Fig. Q3(b), complete the truth table and for the clock cycles shown, sketch the waveform Q 3 Marks



J	K	CLK	Q	Q'
0	0	↑		
0	1	↑		
1	0	↑		
1	1	↑		

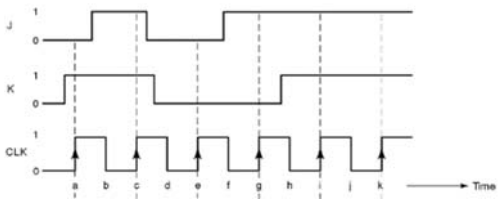


Fig. Q3(b) JK Flip Flop

Q3(c) Fig. Q3(c) shows the state table of a FSM that asserts the output when the input bit stream changes from 0 to 1.

(i) Draw the state transition diagram. 3 Marks

(ii) Derive the minimum SOP terms for the Next State (NS) and the Output 3 Marks

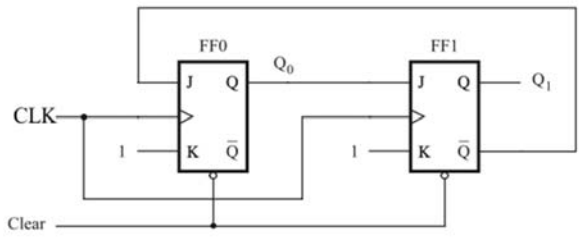
(iii) Draw the circuit to implement the bit stream detector. 2 Marks

	Input IN	Preset State PS	Next State NS	Output OUT
ZERO	0	00	00	0
	1	00	01	0
CHANGE	0	01	00	1
	1	01	11	1
ONE	0	11	00	0
	1	11	11	0

Fig. Q3(c) Finite State Machine State Table

Question 4 (15 Marks)

4(a) The circuit shown in Fig. Q4(a) is driven by square wave clock input. Determine the functional behaviour of the circuit by completing the table shown in Fig. Q4(b). What type of circuit is Fig. Q4(a). 4 Marks



Time interval	FF0			FF1		
	J_0	K_0	Q_0	J_1	K_1	Q_1
Clear	1	1	0	0	1	0
t_1						
t_2						
t_3						
t_4						

Fig. Q4(a) Fig. Q4(b)

Q4(b) Fig. 4(b) shows a four-bit shift register that is used to shift its contents one bit position to right. The data bits are loaded into the shift register in a serial fashion using the I_n input. The contents of each flip-flop are transferred to the next flip-flop at each positive edge of the clock.

(i) Complete the output sequence shown in Fig. Q4(c) 3 Marks

(ii) Why are level-sensitive latches not suitable for this shift register 1 Mark

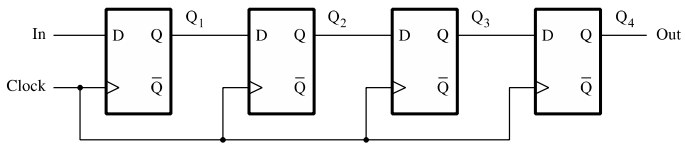


Fig. Q(b) Four-Bit Shift Register

CLK	In	Q_1	Q_2	Q_3	Q_4 = Out
t_0	1	0	0	0	0
t_1	0				
t_2	1				
t_3	1				
t_4	1				
t_5	0				
t_6	0				
t_7	0				

Fig. 4(c) Register Sequence

Q4(c) A 4x4 RAM is built from 16 binary cells (BC), 2x4 decoder and OR gates.

(i) Draw a diagram showing the 4x4 RAM memory arrangement. 5 Marks

(ii) Draw a diagram showing the BC that stores 1 bit 2 Marks