Strathmore
UNIVERSITY

SCHOOL OF COMPUTING AND ENGINEERING SCIENCES
BACHELOR OF BUSINESS & INFORMATION TECHNOLOGY
YEAR 2 - BBIT, CNS
END OF SEMESTER EXAMINATION

CNS 2202/ BBT2201-COMPUTER ORGANIZATION & ARCHTECTURE

DATE: 18Th DECEMBER 2024 **TIME: 10:30-12:30 HOURS**

INSTRUCTIONS

1. **This Examination consists of FIVE questions.**
2. **Answer Question ONE (COMPULSORY) and any other TWO questions.**

QUESTION ONE (30 MARKS)

1. Explain the following terminologies
   i. Computer architecture **(1 Marks)**
   ii. Instruction set **(1 Marks)**
2. Elaborate the distinction between the following terminologies used in computer architecture
   i. RISC and CISC **(4 Marks)**
   ii. RAM and ROM **(4 Marks)**
3. List **four** characteristics of Auxiliary Memory **(4 Marks)**
4. Explain any **four** major features of fourth generation computers: **(4 Marks)**
5. Convert 2561_{16} to its octal equivalent **(3 Marks)**
6. Explain **10** components of a computer architecture system **(5 Marks)**
7. Explain **four** functions of a digital computer **(4 Marks)**

QUESTION TWO (15 MARKS)

1. Explain **five** different types of instruction set in the 8085 CPU with an example opcode **(5 Marks)**
2. Describe **five** types of addressing modes with suitable diagrams and examples. **(10 Marks)**

QUESTION THREE (15 MARKS)

1. State four comparisons between CISC and RISC architectures **(4 Marks)**
2. Explain the purpose of the following registers **(6 Marks)**
    i. Instruction registers
    ii. Program counter
    iii. Memory buffer register
3. Outline four differences between the intel 80885 architecture masked and non-masked interrupts **(2 Marks)**
5. Discuss the cache memory and the different levels in it **(3 Marks)**

QUESTION FOUR (15 MARKS)

1 State and explain two types of buses **(2 Marks)**
2 Explain **five** components of the bus design **(5 Marks)**
3 Explain the following operations with example **(3 Marks)**
    i. ACI
    ii. SUB
    iii. LDAX
4. Write an assembly code for 8-bit addition of two hexadecimal numbers using accumulator in 8085 **(5 Marks)**

QUESTION FIVE (15 MARKS)

1. Draw the logic gate diagram for the NOR and NAND operation **(2 Marks)**
2. With a truth table show the implementation of the following logic circuits **(8 Marks)**

    i. AND gate
    ii. NOT gate
    iii. NAND gate
    iv. OR gate
3. Using a diagram describe the direct mapping cache organization technique **(3 Marks)**
4. Convert the expressions 1110101110_2 to hexadecimal equivalent **(2 Marks)**