Strathmore UNIVERSITY

SCHOOL OF COMPUTING AND ENGINEERING SCIENCES

BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

BEE 2201: DIGITAL ELECTRONICS I

END OF SEMESTER EXAM

Date: 13th March, 2025 **Time:** 08.30 - 11.30

Instructions:

1. This Examination consists of **FIVE** questions
2. Answer **Question ONE (COMPULSORY)** and any other **TWO** questions.

Question 1

a. Convert the following values to their respective forms. (5marks)
   i. 1100.625_{10} to binary
   ii. $3FEE.1CC_{16}$ to decimal
   iii. 1110010.0011_2 to decimal
   iv. 177_{10} to Octal
   v. 110.567_{16} to BCD

b. Draw the truth table for a half subtractor and the circuit diagram from the truth table (4marks)

c. Realize a JK flipflop using the SR flipflop (Draw the truth table and the circuit diagram) (4marks)

d. Implement the following circuit using NOR and NAND gates (4marks)

$$x = (A + B)(B + C)(A + C)$$

e. Subtract $(1110.011)_2$ from $(11011.11)_2$ using basic rules of binary subtraction and verify the result by showing equivalent decimal subtraction. (5 marks)

f. Simplify the following expression $F(A, B, C, D) = \sum m(1,3,4,5,6,7,9,12,13)$ (4marks)

g. Draw the circuit diagram for a Static RAM and explain the working of the circuit. (4marks)

Question 2

Given figure 1 below of a 7-segment decoder, answer the following questions.

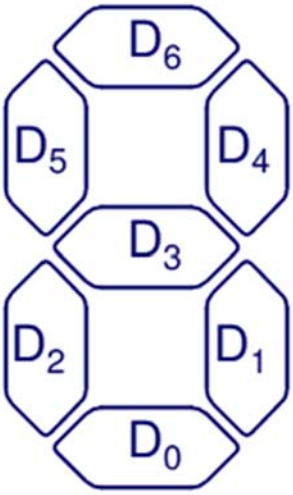

Figure 1

a. Draw the truth table for conversion from binary 0-9 (4marks)
b. Draw the K-maps for all the segments (8marks)
c. Draw the circuit diagram for the 7-segment decoder (3marks)

Question 3

a. State the differences between synchronous and asynchronous sequential circuits (2marks)
b. Draw the circuit diagram and function table for a SR Latch with control input using NAND gates, and explain its working (6marks)
c. Given the figure 2 below answer the following questions.

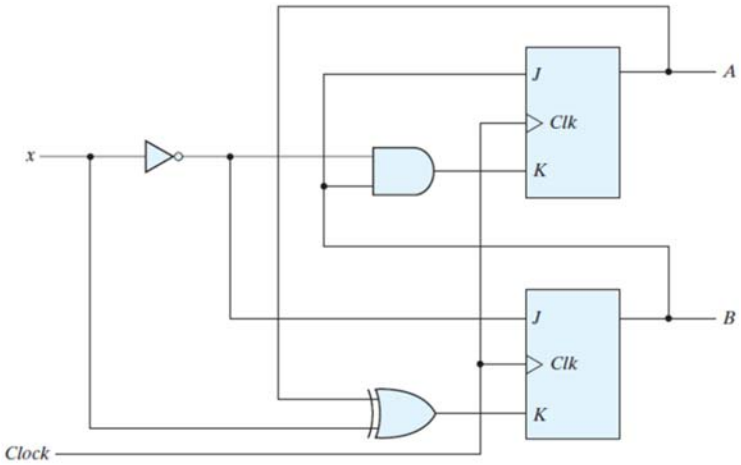

Figure 2

i. Derive the input equations to each flipflop (2marks)
ii. Draw the state table for the above sequential circuit (3marks)
iii. Draw the state diagram for the above sequential circuit (2marks)

Question 4

a. Figure 3 below shows a 4-bit in serial out shift register that is shifted from left. Assuming that the register is initially clear, develop a state table to clearly show the 4-bit pattern after the third clock pulse if we wish to store the nibble 1100. (2marks)

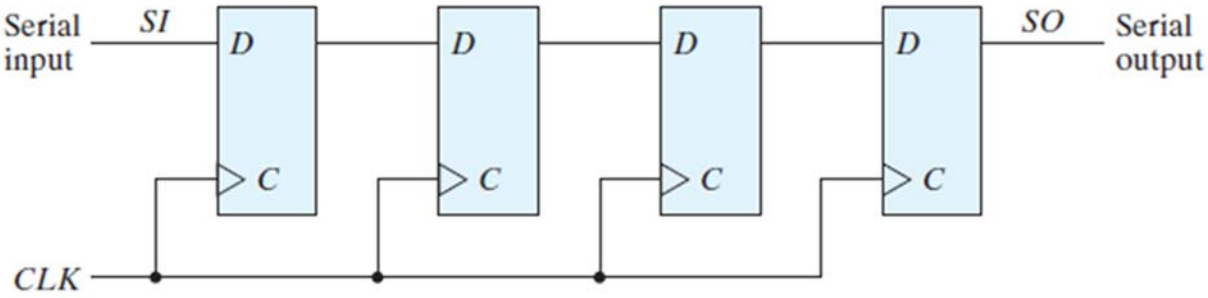

Figure 3

b. Give the differences between a synchronous counter and a ripple counter (4marks)
c. For a 3bit ripple counter using JK flipflops, draw the circuit diagram, truth table and the timing diagram to explain its functionality (9marks)

Question 5

a. Explain the different types of ROMs (3marks)
b. Using diagrams discuss the following types of programmable Logic Configurations.
   i. PROM (2marks)
   ii. PAL (2marks)
   iii. PLA (2marks)
c. Using the following truth table, design a ROM to show address line 3 using a fuse link (3marks)

ROM Truth Table (Partial)

Inputs					Outputs							
I_4	I_3	I_2	I_1	I_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		⋮							⋮			
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

d. Design a counter system with three inputs denoted A, B, C. Presence or absence of an input is represented by 1 and 0 respectively and the output is a two-bit number X_1X_0, representing that count in binary. (3marks)

i. Write the truth table for this circuit.

ii. Find the minimized logic equations for outputs X_1 and X_0;

iii. Draw the corresponding labelled logic diagram for this circuit using basic gates