Strathmore UNIVERSITY

SCHOOL OF COMPUTING AND ENGINEERING SCIENCES

BACHELOR OF ELECTRICAL AND ELECTRONICS ENGINEERING

BEE 4206: MICROPROCESSOR SYSTEMS

END OF SEMESTER EXAM

Date: Monday, 16th March 2026. **Time:** 16.00 - 18.30 Hours

Instructions:

This Examination consists of **FIVE** questions

Answer **Question ONE (COMPULSORY)** and any other **TWO** questions.

Question one [20 Marks]

a) Compare the bus widths (address and data) of the Intel 8086 and 8088 microprocessors, and explain how these differences impact memory addressing capabilities in a practical system design. **4marks**

b) Draw a diagram illustrating the memory mapping for a 1MB address space using the 8086 microprocessor, labeling the address lines (A0-A19) and explaining how segmentation is used to extend beyond 64KB limits. **4marks**

c) Differentiate between the pipelined architecture of the 80286 and the non-pipelined architecture of the 8086, and analyze how this affects instruction execution speed in a multitasking environment. **4marks**

d) Explain the function of the RESET pin on an Intel microprocessor, including a logical sequence of events that occur during a system reset, and discuss potential issues if this pin malfunctions. **4marks**

e) Given a scenario where a system requires expansion from 512KB to 1MB of RAM using additional memory chips, design a diagram showing the address line connections for memory decoding and justify the choice of address bits for chip selection. **4marks**

Question two [20 Marks]

a) Describe the role of the Arithmetic Logic Unit (ALU) in a microprocessor's operation, and evaluate its importance in handling both arithmetic and logical instructions during program execution. **4marks**

b) Explain the interrupt handling mechanism in an 8086 microprocessor, including the difference between maskable and non-maskable interrupts, and provide a logical rationale for prioritizing interrupts in real-time applications. **4marks**

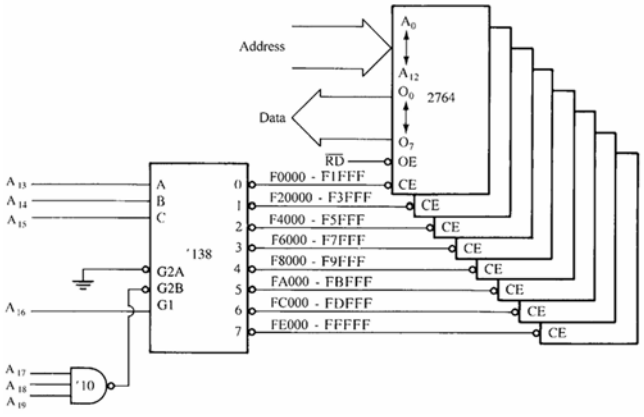
c) Draw a block diagram of the internal architecture of the 8051 microcontroller, labeling key components like the program counter and stack pointer, and analyze how these facilitate efficient subroutine calls. **4 marks**

d) Discuss the function of the ALE (Address Latch Enable) pin in an Intel microprocessor, and explain logically how it enables multiplexing of address and data buses to reduce pin count. **4marks**

e) Evaluate the impact of clock speed on microprocessor performance, using the example of upgrading from a 5MHz to a 10MHz 8086, and justify any trade-offs in power consumption or heat generation. **4marks**

Question three [20 Marks]

a) The diagram below represents a setup for eight 2764 EPROMs. Determine the size of each memory unit in bytes, the total memory size also in bytes, and the word size of each unit. 4marks



b) Write an assembly language code snippet for the 8086 to read data from an I/O port at address 0x300 and store it in the AX register, then explain the logical steps involved in the I/O operation. **4marks**

c) Desing a subroutine in assembly language that configures an I/O port as output and sends a byte value to toggle an LED connected to it, including parameter passing via registers, and justify the use of subroutines for modularity**. 4marks**

d) Analyze a given assembly code segment that performs I/O polling versus interrupt-driven I/O, and evaluate which method is more efficient for a high-speed data acquisition system, providing logical reasoning. **4marks**

e) Explain the function of the IN and OUT instructions in assembly language, and create a simple program that uses them to interface with a keyboard input port, handling potential data ready flags logically. **4marks**

Question four [20 Marks]

a) Distinguish between Isolated I/O and Memory Mapped IO **4marks**

b) Describe what happens to the status flags as a result of the execution of the following program in Intel 8086.

```
MOV AX, 1234H
MOV BX,0ABCDH
CMP AX,BX
```

4marks

c) Draw a flowchart illustrating the logical sequence of handling multiple interrupts in an assembly program, including saving and restoring registers, and evaluate the risks of interrupt nesting if not managed properly. **4marks**

d) Explain the function of the INT pin on a microprocessor and how it triggers software interrupts, then create an assembly routine that uses INT 21h for DOS services like displaying a message. **4marks**

e) As an engineer you are task with configuring the Intel 8255 PPI design the control word that will configure port A as a bidirectional port, port as an interrupt enable port while port C upper is used as the control input port for port A while port C lower is used as the control output port for port B. **4marks**

Question five [20 Marks]

a) Explain the functions of the data bus pins (D_0-D_{15}) in an 8086 microprocessor, and discuss how bidirectional buffering is logically implemented to handle read and write operations. **4marks**

b) Draw a diagram for memory expansion using bank switching in an 8086 system to access 2MB of memory, labeling the address lines and control signals like RD and WR, and explain the switching logic. **4marks**

c) Design an EPROM of size 1M x 16 using the available 128K x 8 memory units . **4 marks**

d) Given a memory map with ROM at 0xF0000-0xFFFFF and RAM at 0x00000-0xEFFFF, draw the address decoding circuit using logic gates and explain how address lines A16-A19 are used for chip selection. **4marks**

e) Evaluate the role of the HOLD and HLDA pins in DMA operations for memory access, and create a logical sequence diagram showing how a DMA controller interacts with the microprocessor during a hold request. **4 marks**