Strathmore UNIVERSITY

SCHOOL OF COMPUTING AND ENGINEERING SCIENCES
BACHELOR OF ELECTRICAL AND ELECTRONICS ENGINEERING
END OF SEMESTER EXAMINATION

BEE 3102: DIGITAL ELECTRONICS II

DATE: 28th October 2024 **Time: 08:00 – 11:00**

Instructions
1. This examination consists of **FIVE** questions.
2. Answer **Question ONE (COMPULSORY)** and any other **TWO** questions.
3. Do not write on the question paper.

QUESTION ONE **(Total:30 Marks)**

a) A particular logic family has V_{OH} = 5 V, V_{OL} = 1 V, V_{IH} = 3.5 V, and V_{IL} = 2 V. Determine its noise margin NM_H and NM_L. (4 Marks)

b) Develop the truth tables for the logic families' circuits in figure 1 and state their respective logic families. (4 Marks)

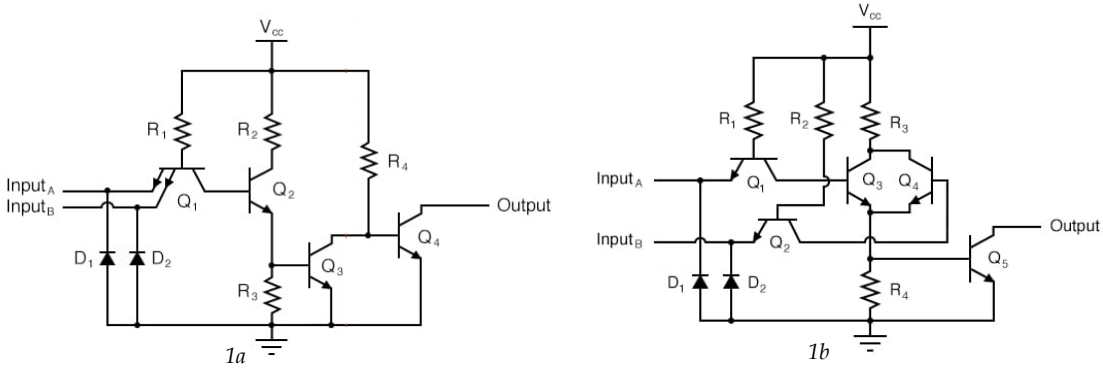

Figure 1

c) Using clearly labelled block diagrams, differentiate between Programmable Read Only Memory (PROM), Programmable Array Logic (PAL), and Programmable Logic Array (PLA). (3 Marks)

d) What is the sequence detected by the sequence detector in figure 2? (3 Marks)

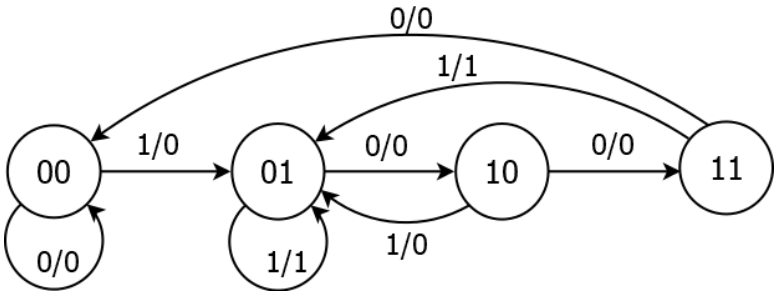

Figure 2

e) A 16-bit Digital-to-Analog Converter (DAC) using a Binary Coded Decimal (BCD) input code has a full-scale output of 9.99V. Calculate the percentage resolution and the output voltage (V_{out}) for an input code of 0110100101010111. (3 Marks)

f) A given sequential network has one input and one output. The output becomes 1 and remains 1 thereafter when at least two zeros and at least two ones have occurred as inputs, regardless of the order of occurrence. Draw a state graph (Moore type) for the network. *Note: 9 states are sufficient and your final state graph should be neatly drawn with no crossed lines.* (4 Marks)

g) A 6-bit D/A converter produces an output voltage of 12 V for an input code of 101010. What will be the value of the output voltage for an input code of 110110? (3 Marks)

h) Illustrate with block diagrams and discuss the following terms as used in Algorithmic State Machines

i. State Box (2 Marks)
ii. Decision Box (2 Marks)
iii. Combinational Box (2 Marks)

QUESTION TWO **(Total: 15 Marks)**

a) Realize a PROM using the following expression. (5 Marks)

$$(a, b, c) = \sum m(0, 1, 3, 5, 7) \; and \; f_2(a, b, c) = \sum m(1, 2, 5, 6)$$

b) Design a 4-bit DAC using binary-weighted resistors and calculate the output voltage for an input code of 1101, given that the reference voltage is 5V. (6 Marks)

i) Draw a clearly labelled schematic diagram for a 2 input CMOS NAND gate. (4 Marks)

QUESTION THREE **(Total: 15 Marks)**

a) Design an overlapping sequence detector to detect 1001 from a data sequence of 100100100100111011 by answering the following questions

i. Draw a state diagram for this detection. (3 Marks)
ii. Develop a corresponding state table and perform the state assignment (2 Marks)
iii. Using JK flip flops, draw the excitation table (4 Marks)
iv. Using K-Maps, minimize the functions of output and flip flop inputs (3 Marks)
v. Draw the circuit diagram using block Diagram of JK flip flops and basic gates (3 Marks)

QUESTION FOUR **(Total: 15 Marks)**

a) Reduce the number of states in state diagram in Figure 2 using;
   i. Partitioning method (4 Marks)
   ii. Implication Tables method (4 Marks)

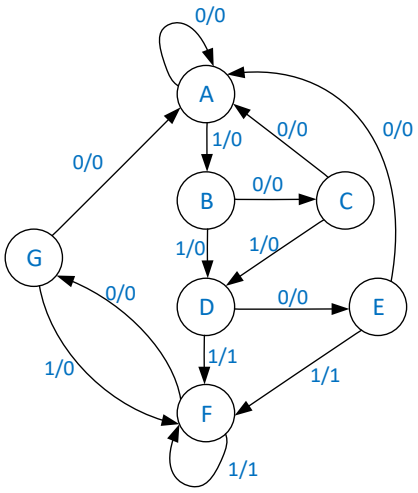

Figure 2

b) Draw a block diagram of Mealy and Moore machines and discuss their differences (4 Marks)

c) Illustrate and discuss the concept of memory decoding (3 Marks)

QUESTION FIVE **(Total: 15 Marks)**

a) A 3-bit Flash ADC is used to digitize an analog input signal. Given a reference voltage V_{REF} is 8V;
   i. Determine the number of comparators required for this Flash ADC. (2 Marks)
   ii. Calculate the voltage resolution of the ADC. (2 Marks)
   iii. Determine the digital output for an analog input voltage of 5.5, 5.8, 3.8, and 4.6 V. (6 Marks)

b) Write a Verilog program for a Full Adder. (5 Marks)